In the Specification:

Please amend the paragraph beginning on page 4, line 30 as follows:

The present invention is based on the recognition that the usage of a flexible bridge for a signal bus between two modules allows to connect all memory modules, and, thus, all memory chips on the memory modules, without stubs, and, therefore, to make signal quality better. Such a stub-less topology can be referred to as SLT topology (SLT=short loop through) in view of the fact that all memory modules are connected ~~connecte~~ in one loop.

Please amend the paragraph beginning on page 7, line 36 as follows:

The embodiment of a memory system according to the invention shown in Fig. 1 comprises a memory circuit board 100 which is named motherboard in the following. A memory contoller 102, a first slot connector 104, a second slot connector 106, a third slot connector 108, a fourth slot connector 110 and a termination resistor 170 [[112 ]]are arranged on the motherboard 100. First, second, third and fourth memory modules 114, 116, 118 and 120 are inserted into the first to fourth slot connectors 104, 106, 108 and 110. Each of the memory modules includes a number of memory chips 130 arranged on a respective memory module board 132.

Please amend the paragraph beginning on page 8, line 36 as follows:

The datea lines 152 on the memory module board 132 exted from the lower end thereof (at which they are connected by the electrical connectors 154 to the data bus portion 150) to the upper end of the memory module board at which same are connected to respective data lines on the flexible bridge 138 so that the flexible bridge 138 forms a third data bus portion. A fourth data bus portion 156 is formed by data lines on the memory module board of the second memory

module 116, and a fifth data bus portion 158 is formed by data lines located on the motherboard 100 and providing electrical connection between the slot connectors 106 and 108. A sixth data bus protion 160 is formed by data lines on the memory module board of the third memory module 118, a seventh data bus portion is formed by the flexible bridge 140, an eighth [[eight ]]data bus portion is formed by data lines 162 on the memory module board of the fourth memory module 120, and a ninth data bus portion 164 is formed by data lines on the motherboard 100 connecting the electrical connectors 154 of the fourth slot connector 110 to a first ends of a termination resistor 170. The second end of the termination resistor 170 is connected to a reference potentional plane 172 of the motherboard 100.